



University of Moratuwa

Wisdom is all wealth

Noise and Interference in Instrumentation

Part 6 – Best Practices for PCB Design

Anton F. P. Van Putte, Electronic measurement systems, Taylor & Francis, 2nd Edition

M. M. S. Anand, Electronic instruments and Instrumentation Technology, PHI

John G Webster, Medical Instrumentation- Application and Design, John Wiley & Sons, 4th Edition

R.S. Khandpur, Handbook of biomedical instrumentation, Tata McGraw-Hill, 3rd Edition

PCB Design Considerations in Instrumentation

- Analog paths and sensitive nodes:
 - Keep analog signal paths short.
 - Separate analog and digital signals - Keep analog and digital portions separate.
 - Keep inputs and outputs separate and shield sensitive parts if needed.
 - Keep inputs away from unwanted outputs – prevents feedback, oscillation.
 - Parallel components can electromagnetically couple – crosstalk.
 - Do not route sensitive nodes under or between other components.
- Grounding:
 - Provide good ground return paths
 - High frequency bypassing
 - Minimize inductance (vital for high-speed circuits)
 - Maintain effective ground plane.
 - Fill void areas on signal layers with ground fill.
- Power:
 - Power entry better near the outputs - This way, supply currents don't flow near the inputs to amplifying stages.
 - Pay close attention to connecting AGND and DGND
- General:
 - Consider thru-hole interaction – they interact with every layer in a multi-layer design.
 - Surface mount parts have less inductance, but the via placement still sets the loop.

PCB Layout Process

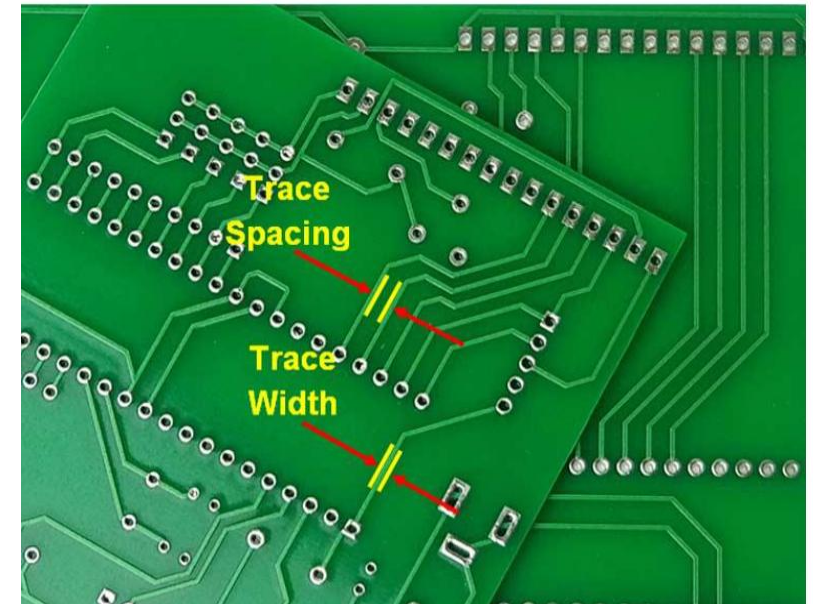
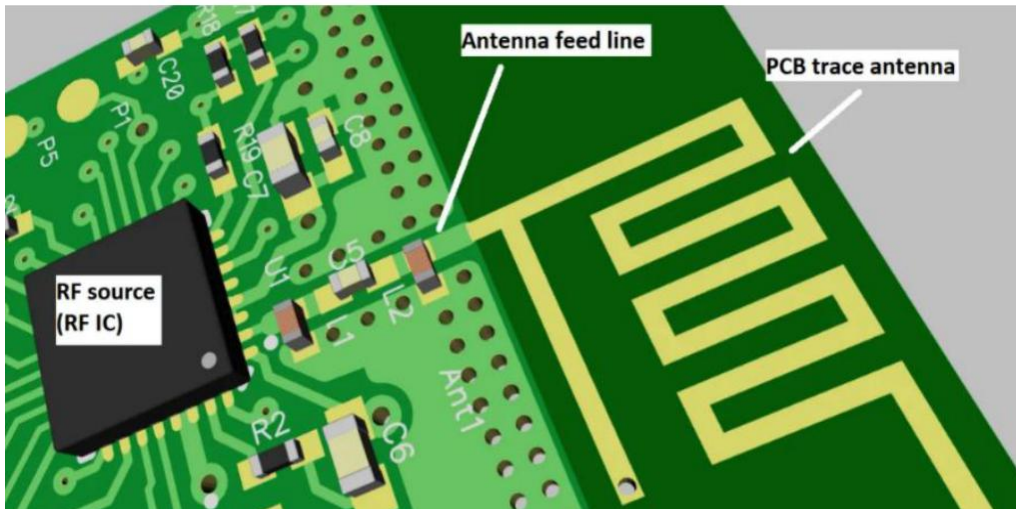
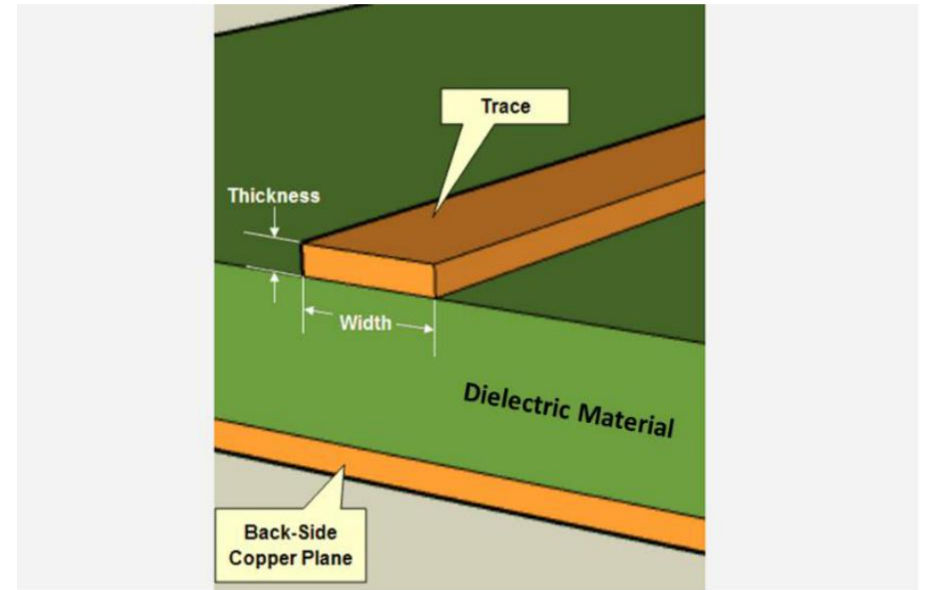
- Review the schematic and mark sensitive areas, sensitive analog paths, EMI and other interference sources, heat sources, etc.
- Fix connector positions and plan part placement before routing.
 - Spend considerable effort in planning (part placement and desired routing paths)
 - Prioritize the analog portion.
 - Power routing and planes.
 - Bypass caps and other critical components.
 - Choose packages that make the layout easier (Ex: SMD for short connections)

Crosstalk

- Crosstalk refers to unwanted transfer of signals between adjacent conductors.
 - Could be due to capacitive or inductive coupling.
- Crosstalk is mostly visible in
 - Parallel signal paths
 - High-speed data lines
- Crosstalk can be mitigated by:
 - Increasing spacing between conductors
 - Using twisted pair cables
 - Differential signaling

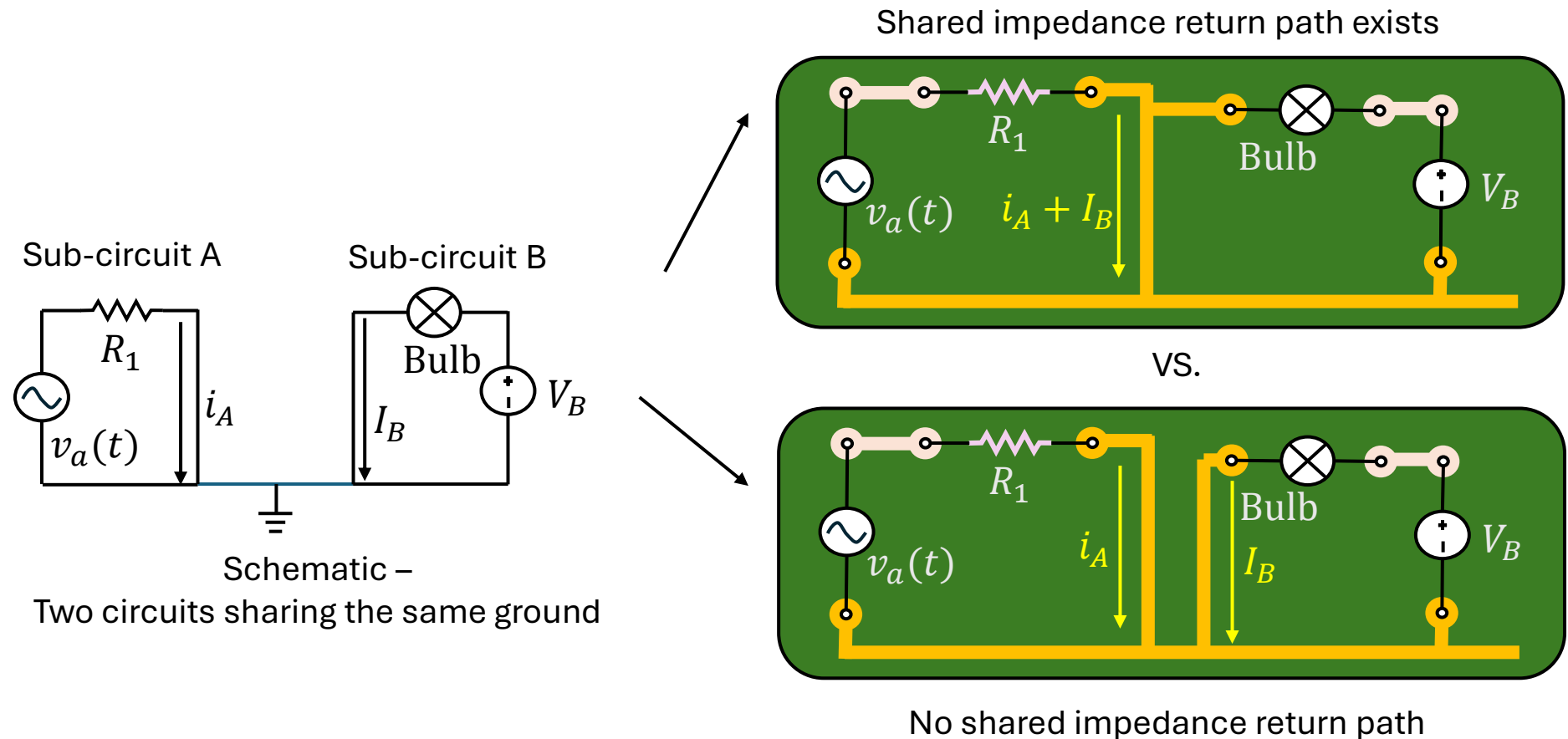
Traces in PCB

- Traces can act like antennas.
 - Traces have transmission line properties:
 - Inductance
 - Resistance
- Traces for power should be wide.
- Connect and terminate effectively (vias)



Mitigating shared ground connections

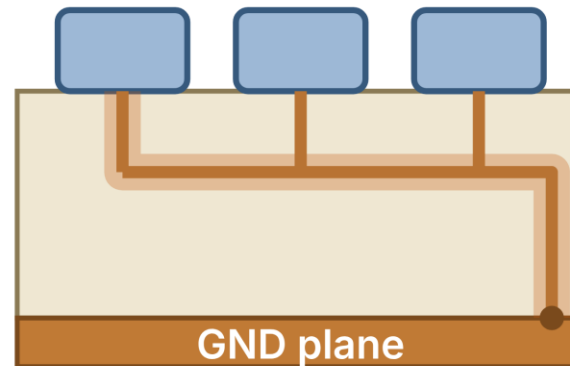
- Shared ground connections can create conductive coupling between subcircuits.
- These can make the ground reference of sensitive circuits fluctuate.



Mitigating shared ground connections

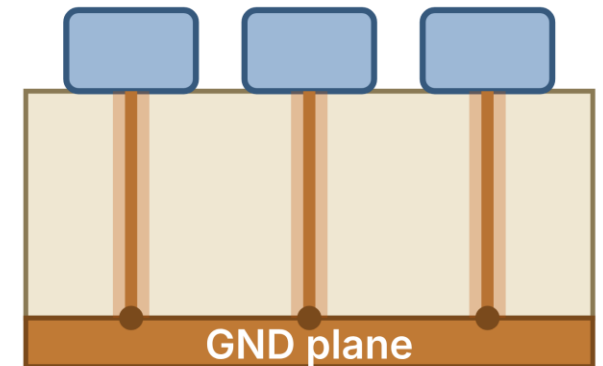
- Shared ground connections can create conductive coupling between subcircuits.
- These can make the ground reference of sensitive circuits fluctuate.

× **Avoid**



long shared return
→ larger ground loop,
shared impedance

✓ **Preferred**



direct via per part
→ shortest return,
minimal loop

Shielding

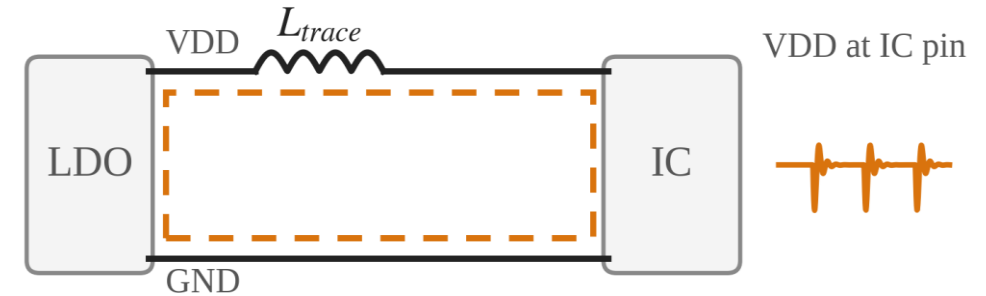
Guard Rings

- Contaminants, moisture, or high-voltage traces on a PCB cause stray nanoampere currents to leak across the board surface.
 - If this leakage reaches a highly sensitive, high-impedance input node, it corrupts the signal.
- To mitigate this, a dedicated copper trace (Guard Ring) is implemented around the sensitive node.
 - Passive guard rings are simply grounded so that it acts as a shield against capacitive coupling.
 - Active guard rings are driven by an op-amp buffer to the exact same voltage as the sensitive input trace.
 - Because the electrical potential between the ring and the input node is identical, the voltage difference is zero.
 - $\therefore$ By Ohm's Law, zero leakage current can cross the gap.
 - Stray current leaking from external noise sources hits the guard ring first and is safely shunted away through the low-impedance op-amp output before it ever reaches the critical signal.

Decoupling (Bypass) Capacitors

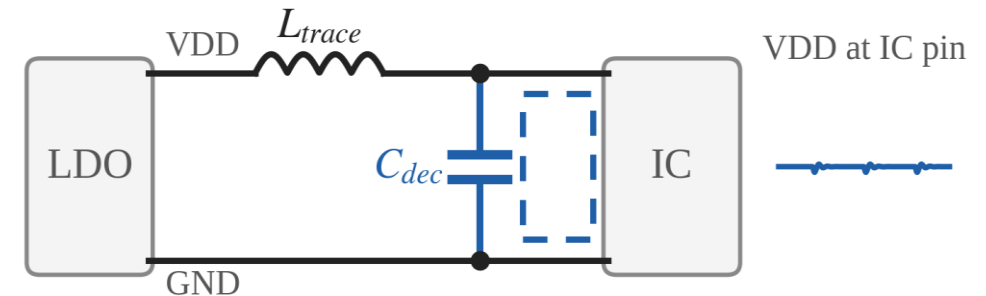
- ICs draw current in short, sharp pulses whenever they switch (logic, MCUs, ADCs, even op-amps).
 - The supply reaches the IC through traces with inductance:
 - Ex: 10 nH and 100 mA in 1 ns $\rightarrow$ a 1 V dip on the IC supply.
- A decoupling capacitor from the supply pin to ground, right next to the IC, is a local charge reservoir:
 - Fast current pulses come from the capacitor through a tiny loop and the regulator only has to top it up slowly.
 - It decouples circuits in both directions:
 - Keeps the IC's switching noise off the shared supply rail,
 - Shunts rail noise to ground before it reaches the IC (adds to its PSRR)
 - Low impedance at high frequency.

Without decoupling



large loop through the trace inductance

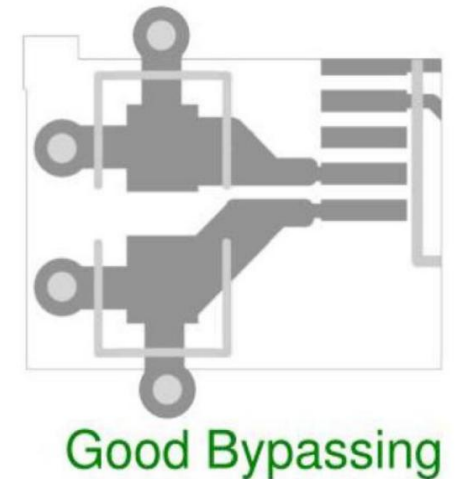
With a decoupling capacitor



small loop

Choosing and Placing Decoupling Capacitors

- Add a 100 nF ceramic capacitor at every supply pin.
 - 1–10 μ F bulk capacitor per rail or IC group, for slower, larger current demands
 - For the assignment, consider adding 100 nF at every IC supply pin:
 - INA, ADC, MCU and LDO outputs (plus any datasheet-specified values)
 - ADC reference pin needs its own decoupling (datasheet value): reference noise goes straight into every sample.
 - AVDD capacitors return to AGND, DVDD capacitors to DGND.
- Placement matters more than value:
 - DO NOT have vias between bypass caps and active device
 - A via adds inductance – defeats the whole point of the capacitor to provide a low inductance path for fast current requirements.
 - Route vias into the bypass caps and then into the active component.
 - The wider the traces the better.
 - The closer the better.
 - Ensure Bypass caps are on same layer as active component for best results.

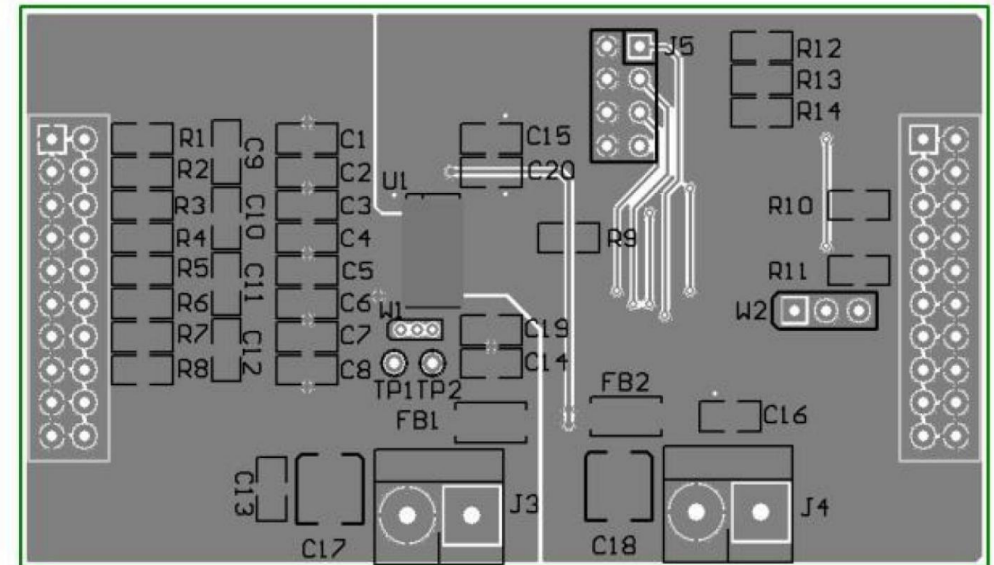


Splitting the PCB

- Partition the PCB into distinct Analog and Digital regions whenever the layout allows.
 - Place analog and digital parts in separate regions of the board
- Split the ground plane only if necessary, a continuous ground is often the better choice.
 - Splitting it can force long return detours
 - Split only if necessary, and then join the grounds at one point (typically under the ADC)

Analog

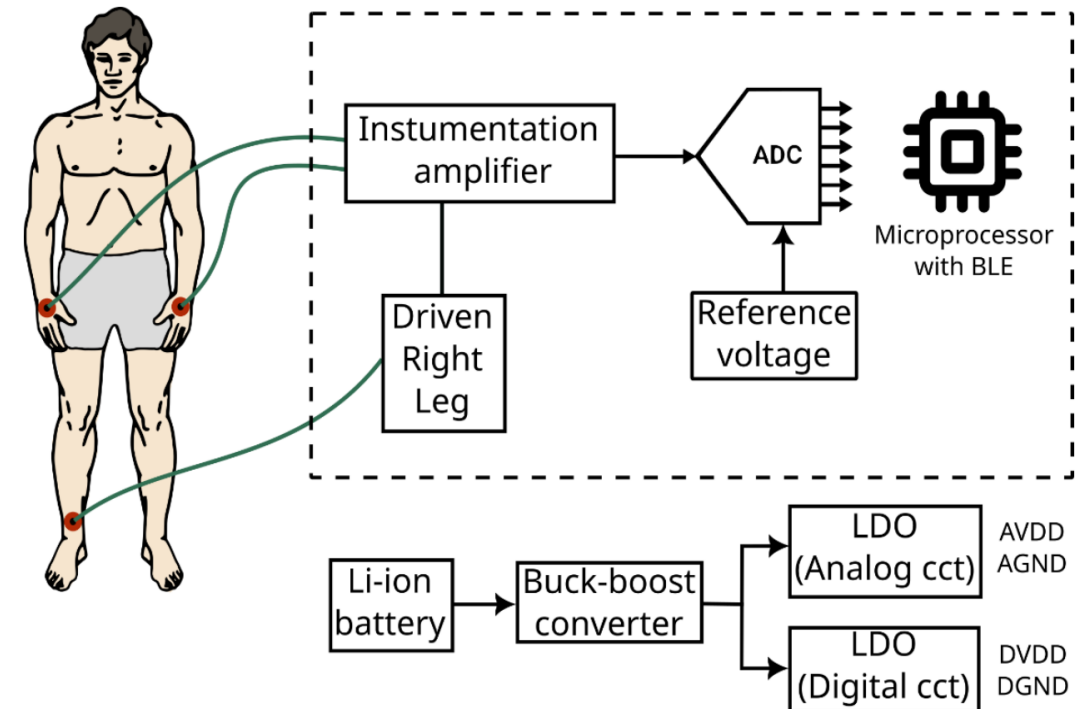
Digital



Assignment

Battery powered wearable ECG signal acquisition device

- Group assignment: 2 students per group
- The assignment aims at evaluating how well you can select and place components and design the layout of the PCB to minimize noise and obtain clean ECG signals.
 - You can add additional components (ex: Filters) if needed but the blocks shown are mandatory.



Assignment

Battery powered wearable ECG signal acquisition device

- Questions:

- Why buck-boost? Why not just buck or boost?
 - Li-ion cell voltage can range from 4.2 V when fully charged, to about 3 V when fully discharged.
 - If we need to maintain 3.3 V, we first need to step down while battery is fully charged but then step up when the battery is severely discharged.
- Why do we need a separate ADC instead of using the one inside the microcontroller?
 - MCU ADC is fine but it has a clock, BLE RF, etc. - these could couple into to the ADC measurements.
 - Instead, we have a separate ADC in the quiet analog area.
 - Resolution versus DC offset:
 - Each electrode–skin interface has a half-cell potential, and the difference between two electrodes can be ≈ 300 mV DC.
 - That's 300 times larger than the 1 mV ECG riding on top of it.
 - A 12-bit MCU ADC with a 3.3 V range has a step size of $q = \frac{3.3}{2^{12}} \approx 0.8$ mV $\therefore$ the whole ECG is about 1 LSB.
 - Getting 1 μ V resolution at the input needs a front-end gain of ~ 800 - At that gain the DC offset saturates the amplifier.
 - You'd need AC coupling, high-pass filters and several gain stages, each adding noise, parts and slow recovery after motion.
 - A 24-bit ADC has a much smaller step size, hence a front-end gain of about 6 is sufficient.
 - Under what conditions would the MCU's ADC be good enough?
 - heart rate only, with an analog front end that already provides gain and high-pass filtering.

Assignment

Battery powered wearable ECG signal acquisition device

- More questions:
 - Why the emphasis on the reference voltage?
 - If this fluctuates, all digitized signals will fluctuate.
 - Why another linear regulator after a switching regulator?
 - The buck-boost leaves tens of mV of switching ripple at 1–2 MHz.
 - An ECG signal may only be 1 mV!
 - The linear regulator cleans up the switching ripple by attenuating the ripple by its PSRR
 - $v_{out_{ripple}} = v_{in_{ripple}} \times 10^{-\frac{PSRR}{20}}$
 - 20 mV with 40 dB of PSRR at 1 MHz leaves 0.2 mV
 - PSRR is frequency dependent – Check regulator datasheet – Usually high at low frequencies.
 - At MHz, PSRR drops - Choose such that it has high PSRR at the switching frequency of the chosen buck-boost converter.
 - Why LDO?
 - Battery powered => keep drop-out voltage as low as possible.

Assignment

Battery powered wearable ECG signal acquisition device

- More questions:
 - Why two LDOs?
 - Two LDOs isolate analog from digital current:
 - MCU and BLE draw current in **pulses** (ΔI).
 - Through a shared impedance Z (A single LDO for both analog and digital sides), this gives $\Delta V = \Delta I \cdot Z$ on that rail.
 - If there was only a single shared LDO, a 10 mA burst through 0.1Ω puts 1 mV straight onto the analog supply.
 - With a separate analog LDO, its PSRR (about 60 dB at low frequency) reduces that to about $1 \mu\text{V}$.
 - This keeps digital return currents and supply noise out of the analog front end.
 - BLE bursts repeat every 7.5–100 ms (10–133 Hz):
 - This itself is inside the ECG band.
 - Therefore, filtering can't remove them.

